FIG. 1

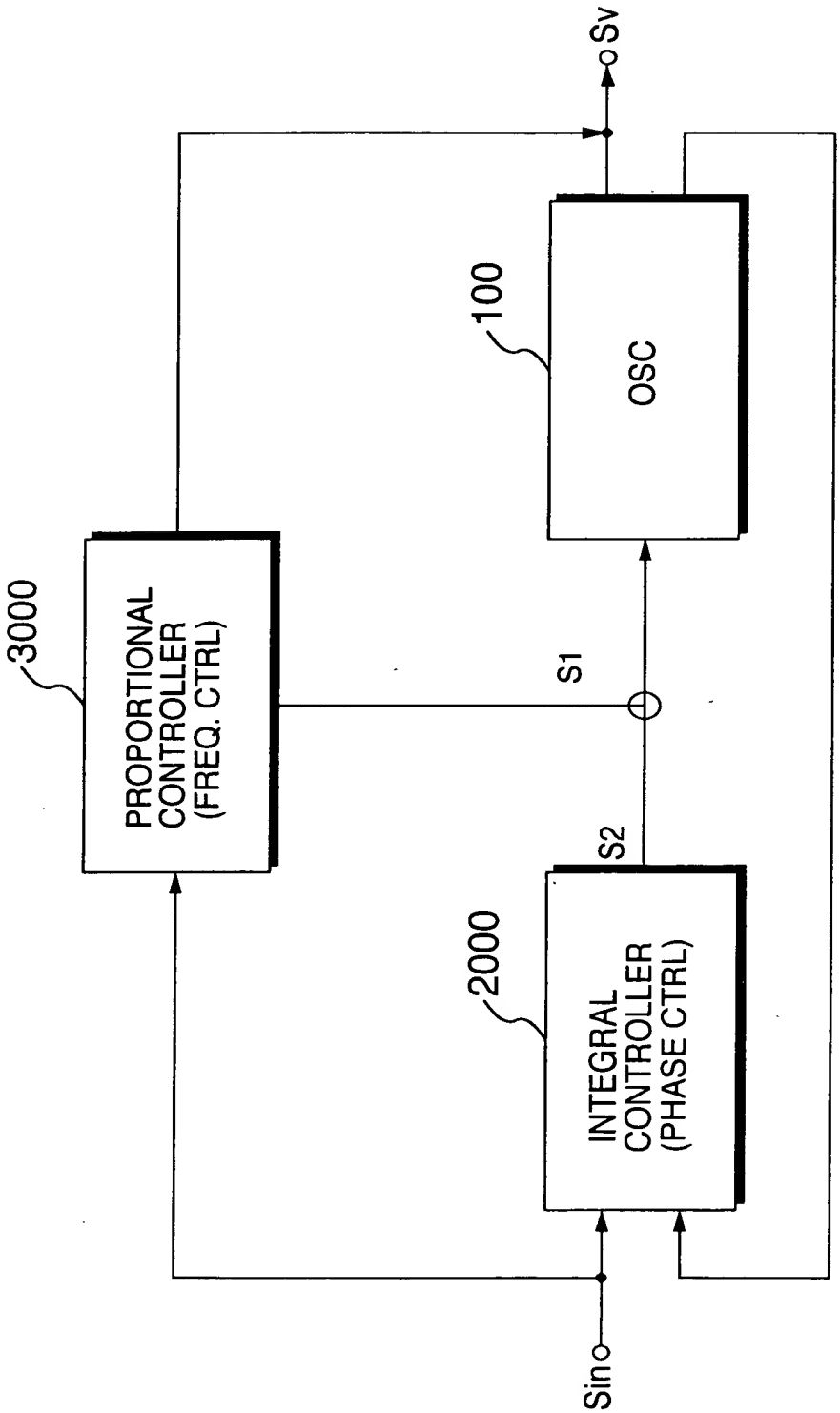
Sv
100
OSC
3000
PROPORTIONAL CONTROLLER (FREQ. CTRL)
S1
S2
2000
INTEGRAL CONTROLLER (PHASE CTRL)
Sin

FIG. 2

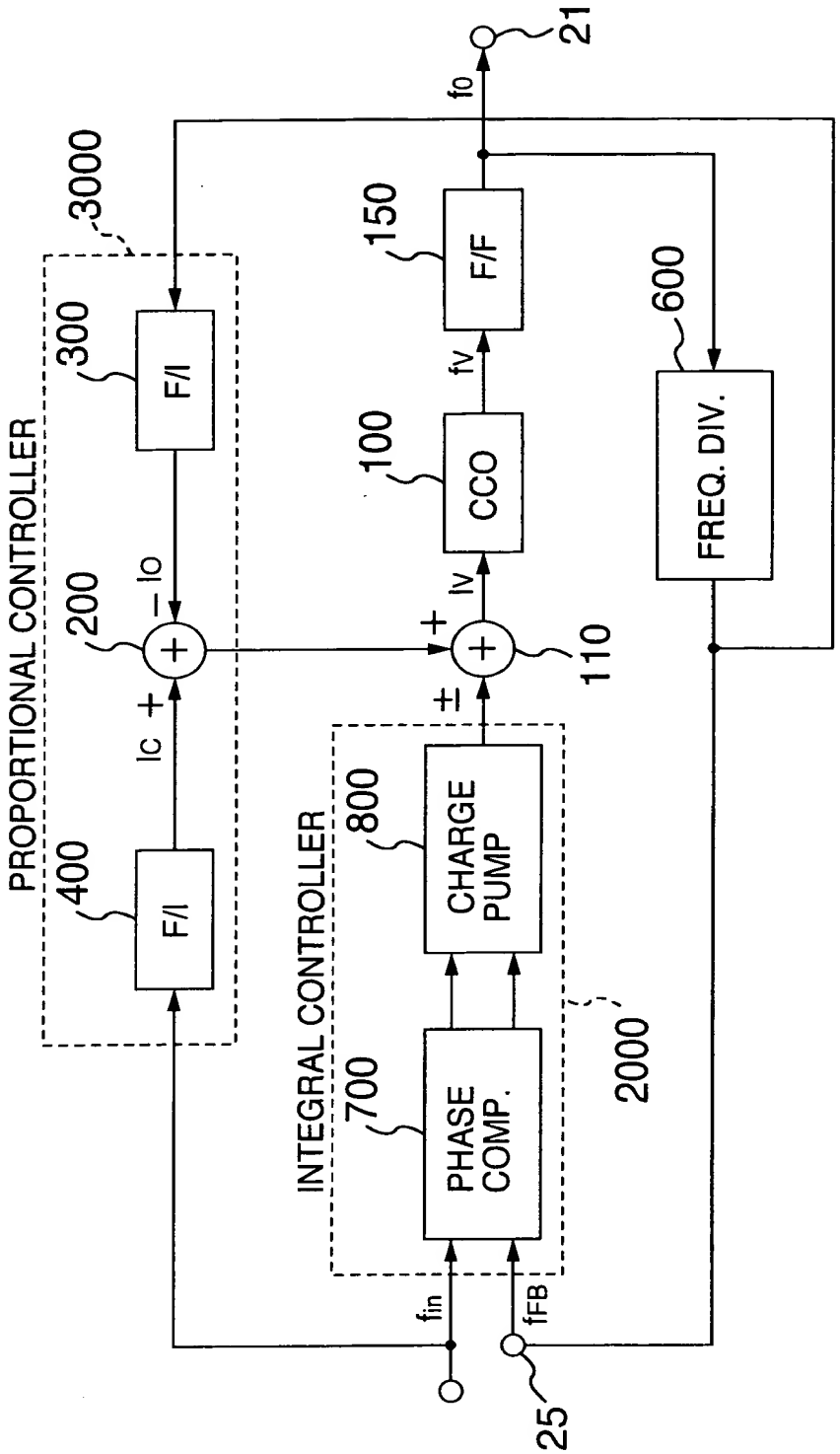
21
fo
3000
150
F/F
600
300
F/I
100
CCO
FREQ. DIV.
PROPORTIONAL CONTROLLER
200
− Io
fv
Iv
+
110
Ic +
±
INTEGRAL CONTROLLER
800
CHARGE PUMP
400
F/I
700
PHASE COMP.
2000
fin
fFB
25

FIG. 3

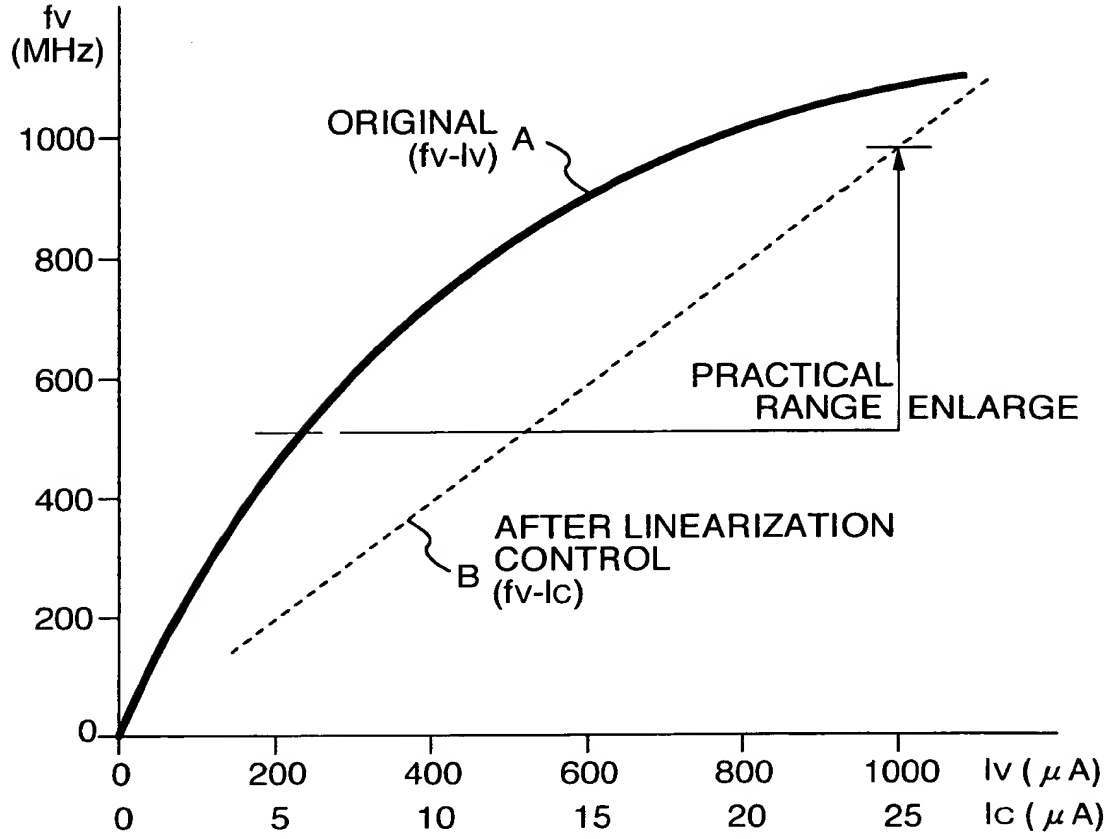
fv
(MHz)
1000
800
600
400
200
0
ORIGINAL
(fv-Iv)
A
PRACTICAL
RANGE
ENLARGE
AFTER LINEARIZATION
CONTROL
(fv-Ic)
B
0
200
400
600
800
1000
Iv (μA)
0
5
10
15
20
25
Ic (μA)

FIG. 4

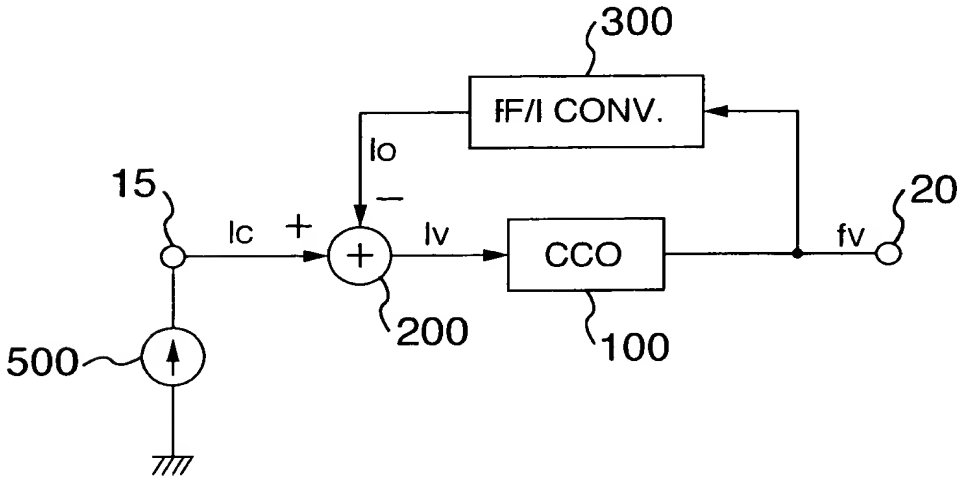
300
fF/I CONV.
Io
15
Ic
+
−
Iv
CCO
fv
20
200
100
500

FIG. 5

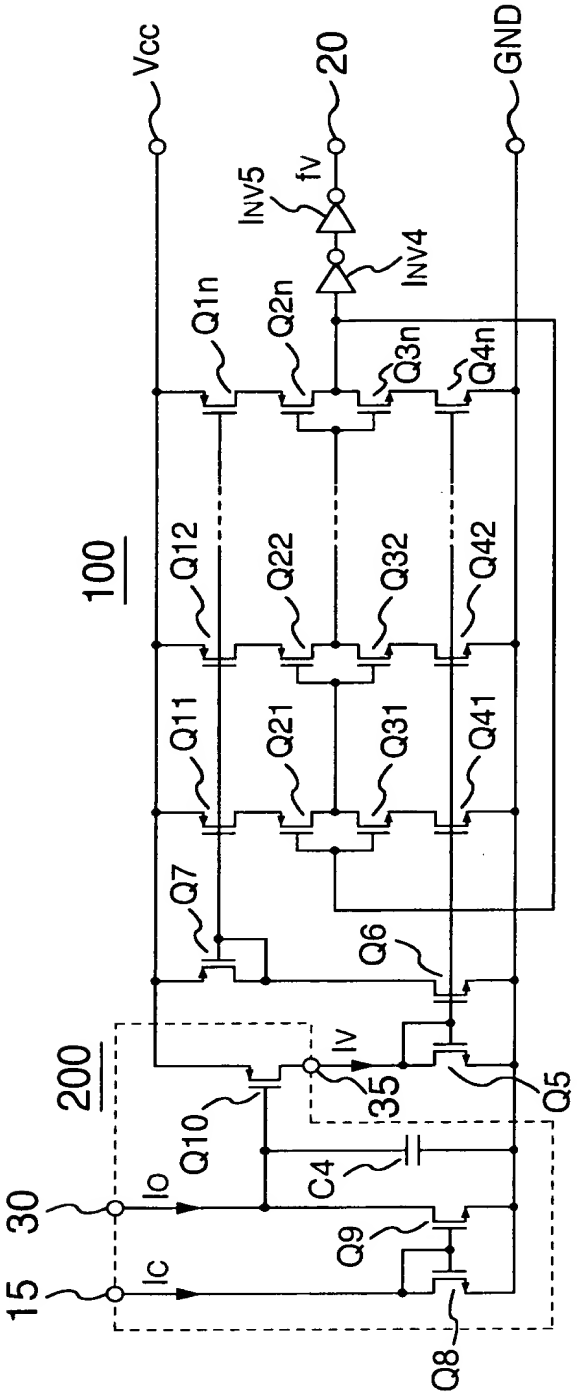
Vcc
GND
20
INV5
fv
INV4
Q1n
Q2n
Q3n
Q4n
100
Q12
Q22
Q32
Q42
Q11
Q21
Q31
Q41
Q7
Q6
200
Iv
35
Q5
Q10
C4
30
Io
Q9
15
Ic
Q8

FIG. 6

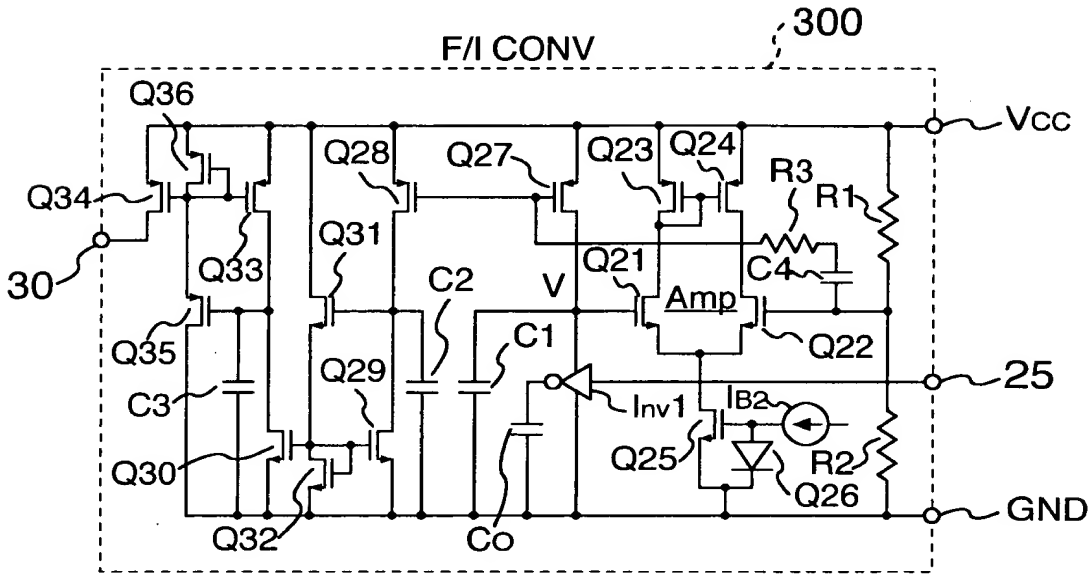
300
F/I CONV
Q36
Vcc
Q28
Q27
Q23
Q24
R3
R1
Q34
Q31
Q21
C4
30
Q33
C2
V
Amp
Q35
C1
Q22
Q29
25
C3
Inv1
IB2
Q25
R2
Q30
Q26
GND
Q32
Co

FIG. 8

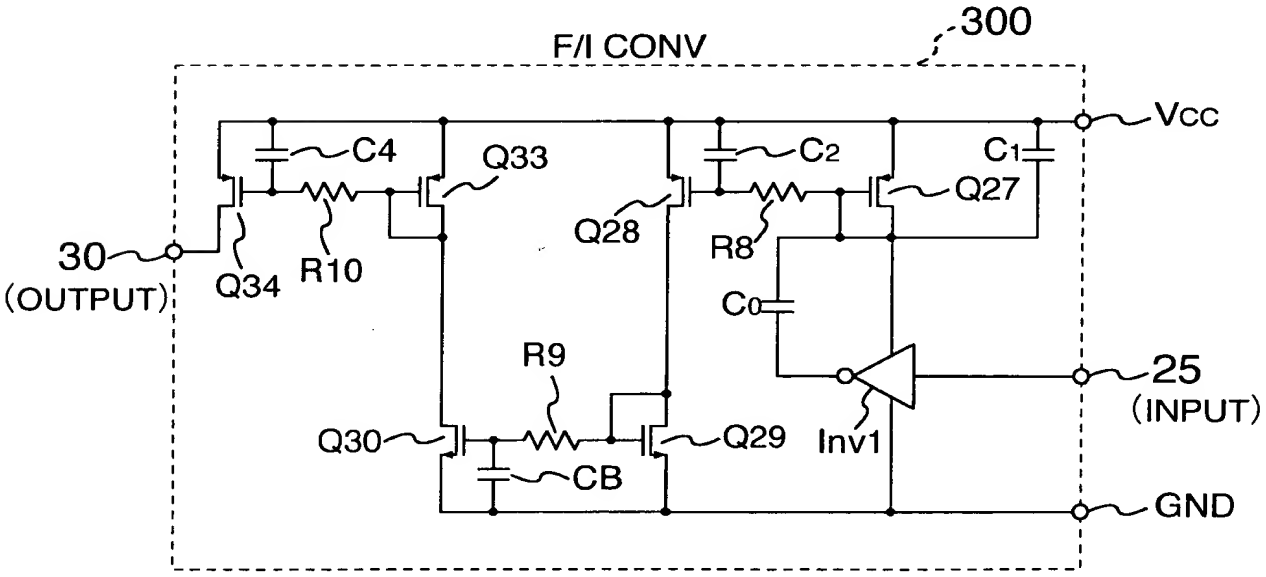
300
F/I CONV
Vcc
C4
Q33
C2
C1
Q27
Q28
R8
30
(OUTPUT)
Q34
R10
Co
R9
25
(INPUT)
Q30
Q29
Inv1
CB
GND

FIG. 7A

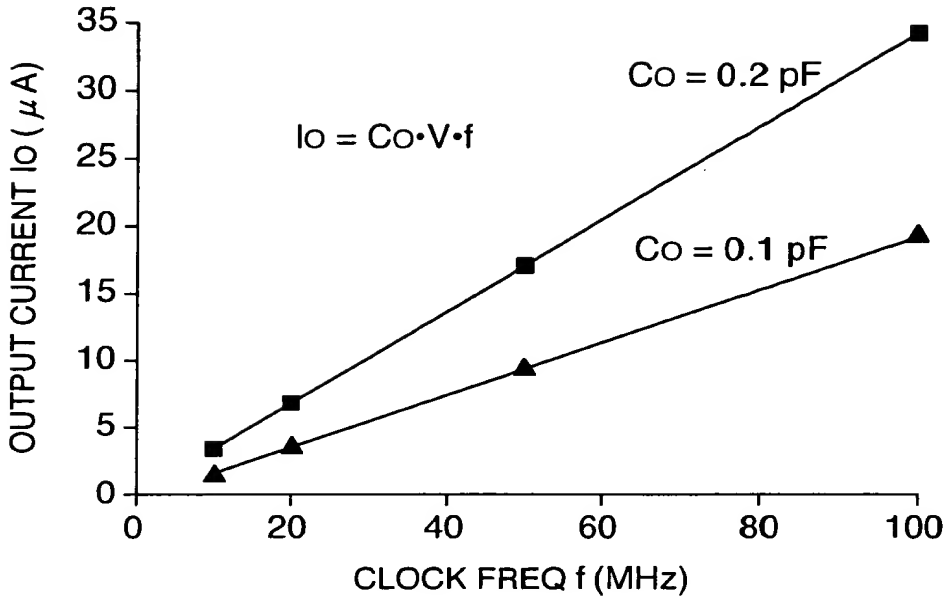
35
30
25
20
15
10
5
0
OUTPUT CURRENT Io (μA)
Io = Co•V•f
Co = 0.2 pF
Co = 0.1 pF
0
20
40
60
80
100
CLOCK FREQ f (MHz)

FIG. 7B

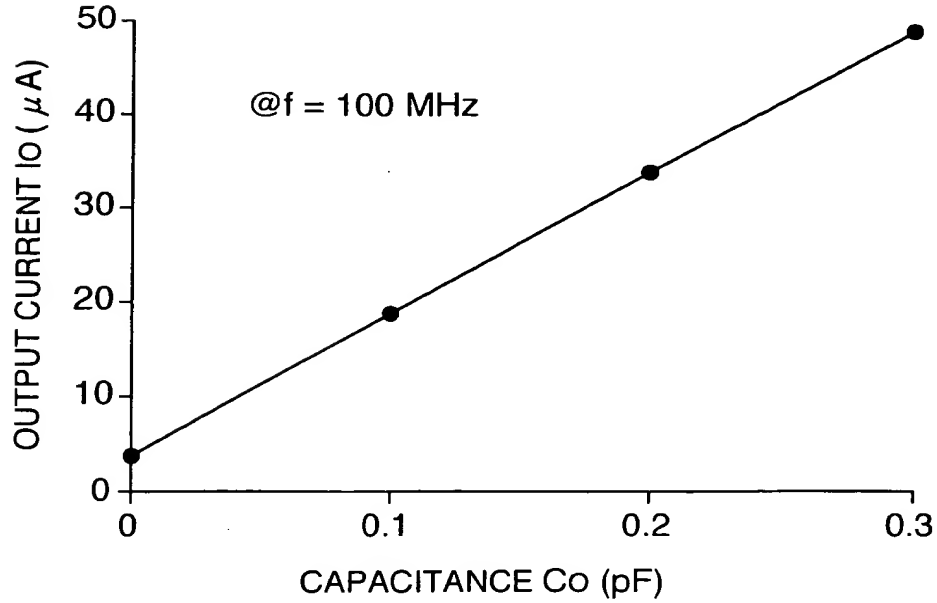
50
40
30
20
10
0
OUTPUT CURRENT Io (μA)
@f = 100 MHz
0
0.1
0.2
0.3
CAPACITANCE Co (pF)

FIG. 9

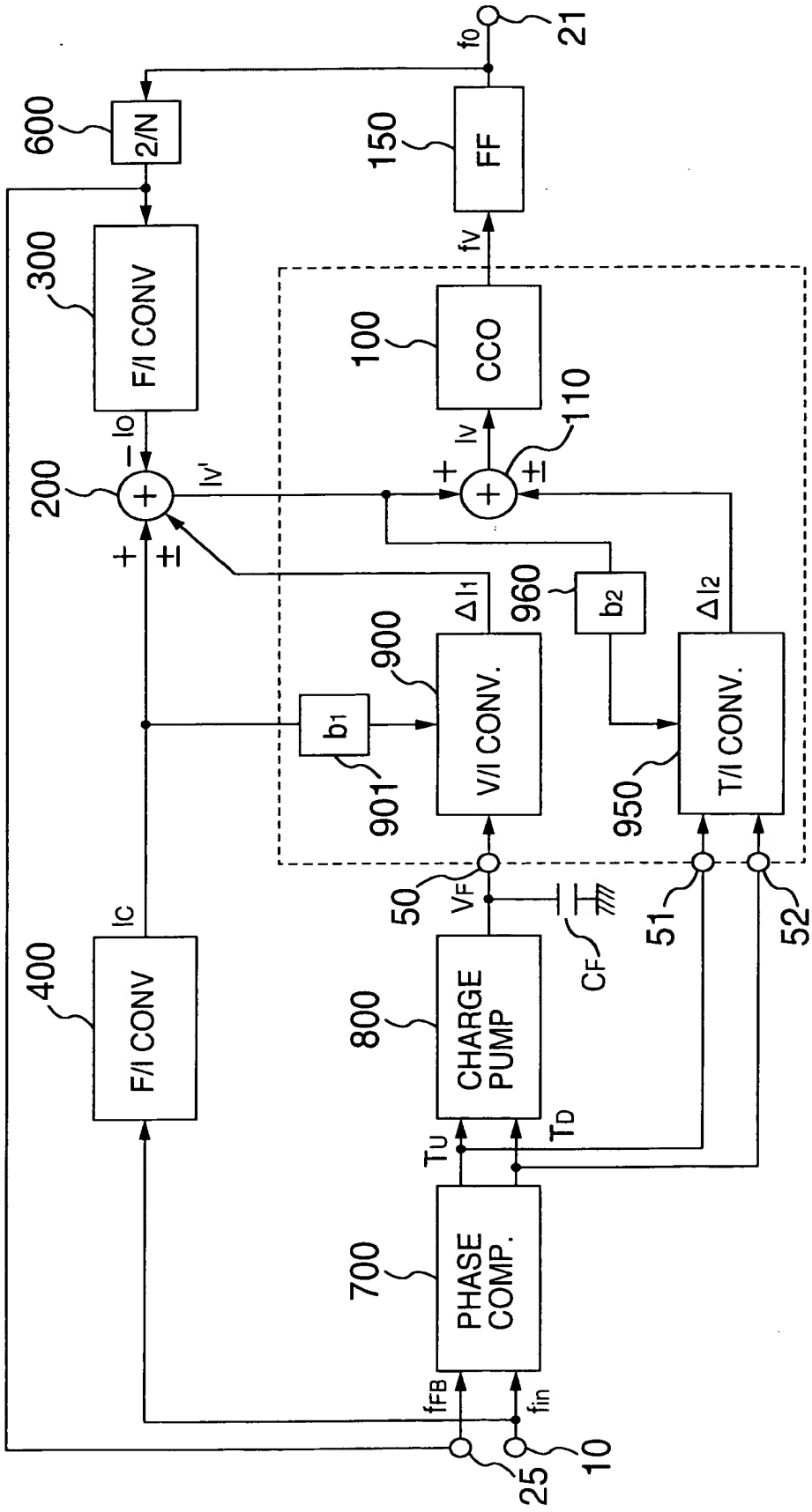
fo
21
600
2/N
150
FF
300
F/I CONV
fV
100
CCO
110
Io
Iv
200
Iv'
+
±
Δl1
960
b2
Δl2
900
b1
V/I CONV.
T/I CONV.
901
950
50
VF
51
52
CF
Ic
400
F/I CONV
800
CHARGE PUMP
TU
TD
700
PHASE COMP.
fFB
fin
25
10

FIG. 10

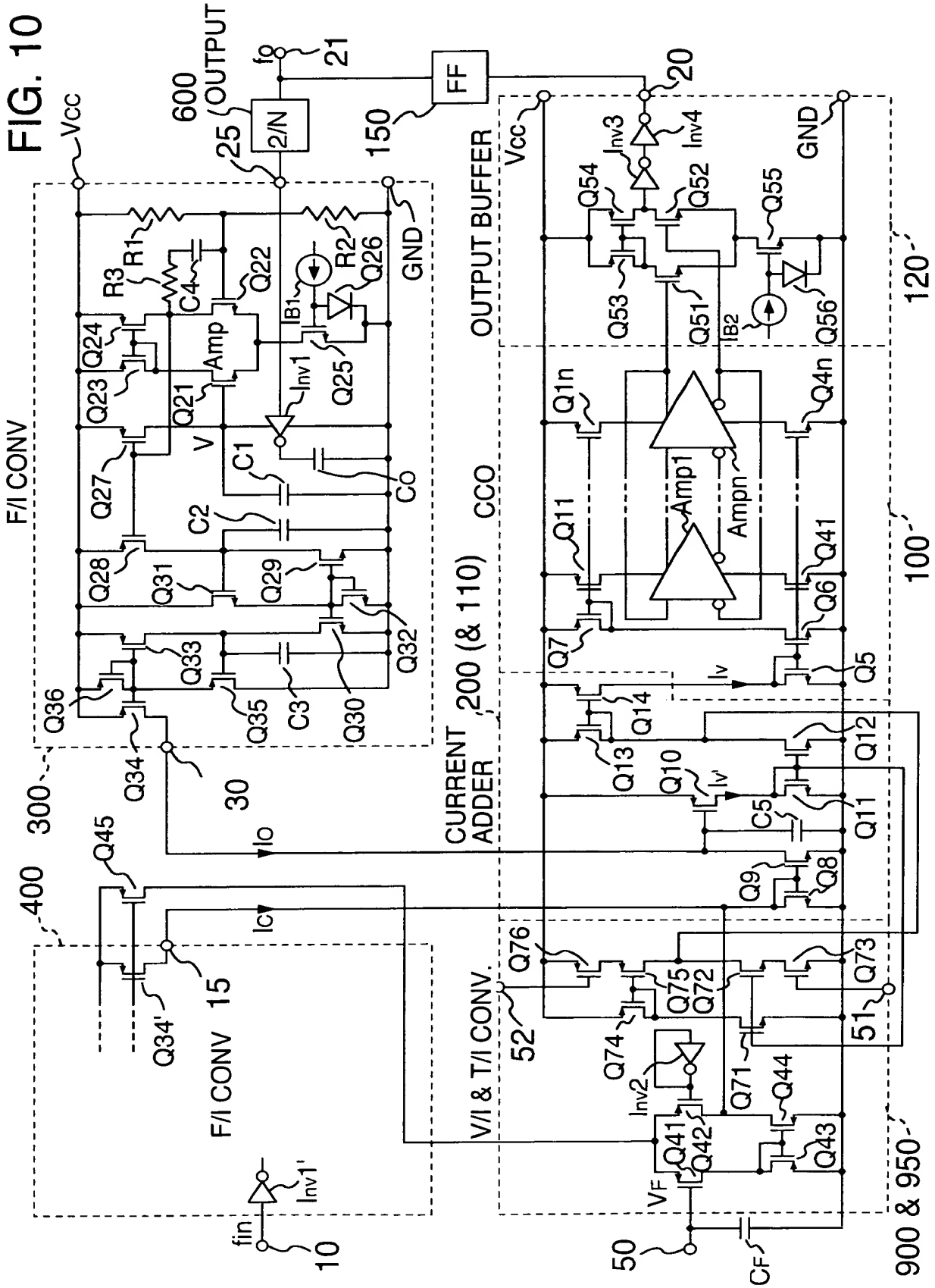
Vcc
600
OUTPUT
25
2/N
fo
21
FF
150
20
F/I CONV
R1
R3
C4
Q22
R2
Q26
GND
IB1
Q24
Amp
Inv1
Q25
Q23
Q21
V
C1
Co
Q27
C2
Q28
Q31
Q29
Q32
Q36
Q33
Q35
C3
Q30
Q34
300
30
Io
CURRENT ADDER
200 (& 110)
CCO
OUTPUT BUFFER
Vcc
Inv3
Inv4
GND
Q54
Q52
Q55
Q53
Q51
IB2
Q56
Q1n
Q4n
Amp1
Ampn
Q11
Q41
Q6
Q7
Iv
Q5
Q14
Q13
Q10
Iv'
Q12
C5
Q11'
Q9
Q8
120
100
400
Q45
Ic
Q34'
F/I CONV 15
Q76
Q75
Q72
Q73
52
V/I & T/I CONV.
Q74
Inv2
Q71
Q44
51
Q41
Q42
Q43
VF
Inv1'
fin
10
50
CF
900 & 950

FIG. 11

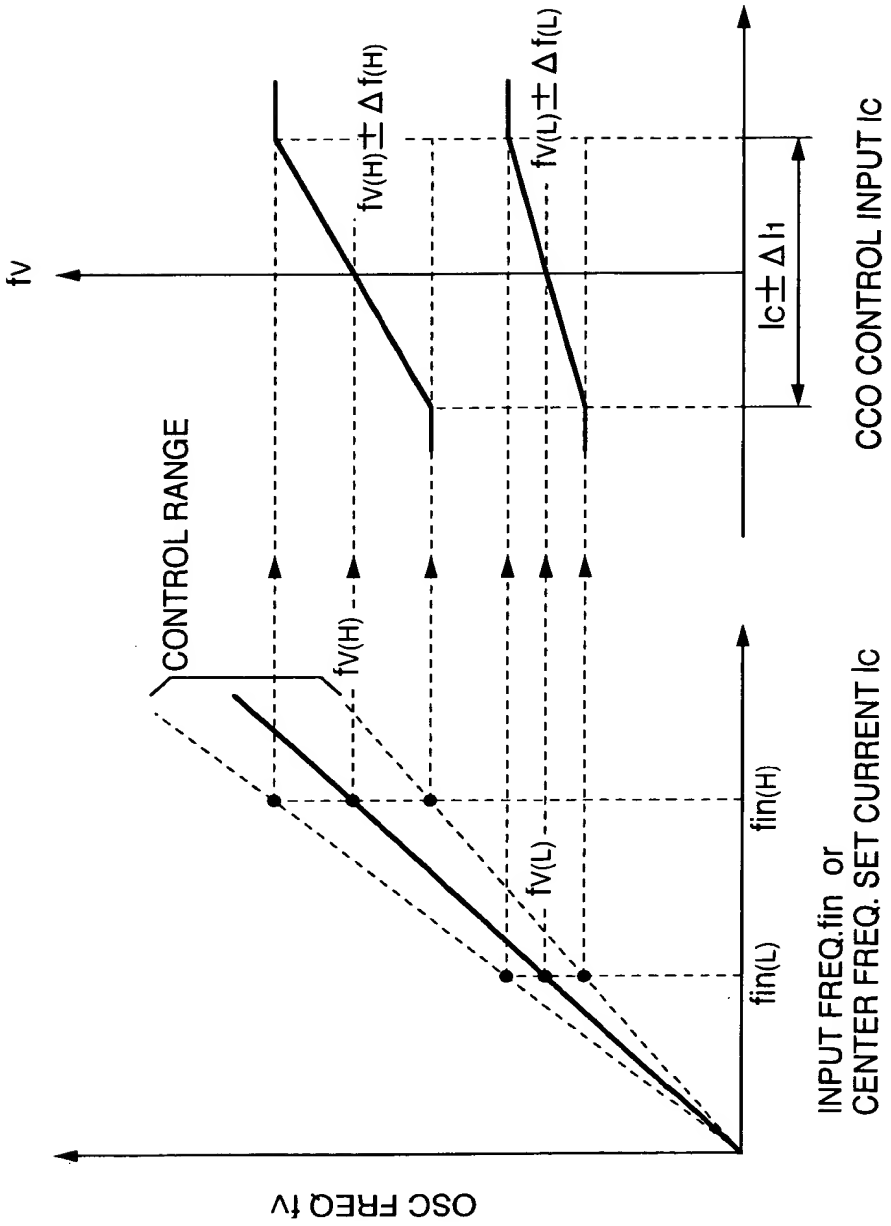
fv
fV(H)± Δ f(H)
fV(L)± Δ f(L)
Ic± Δ I1
CCO CONTROL INPUT Ic
CONTROL RANGE
fV(H)
fV(L)
fin(H)
fin(L)
INPUT FREQ.fin or
CENTER FREQ. SET CURRENT Ic
OSC FREQ fv

FIG. 12

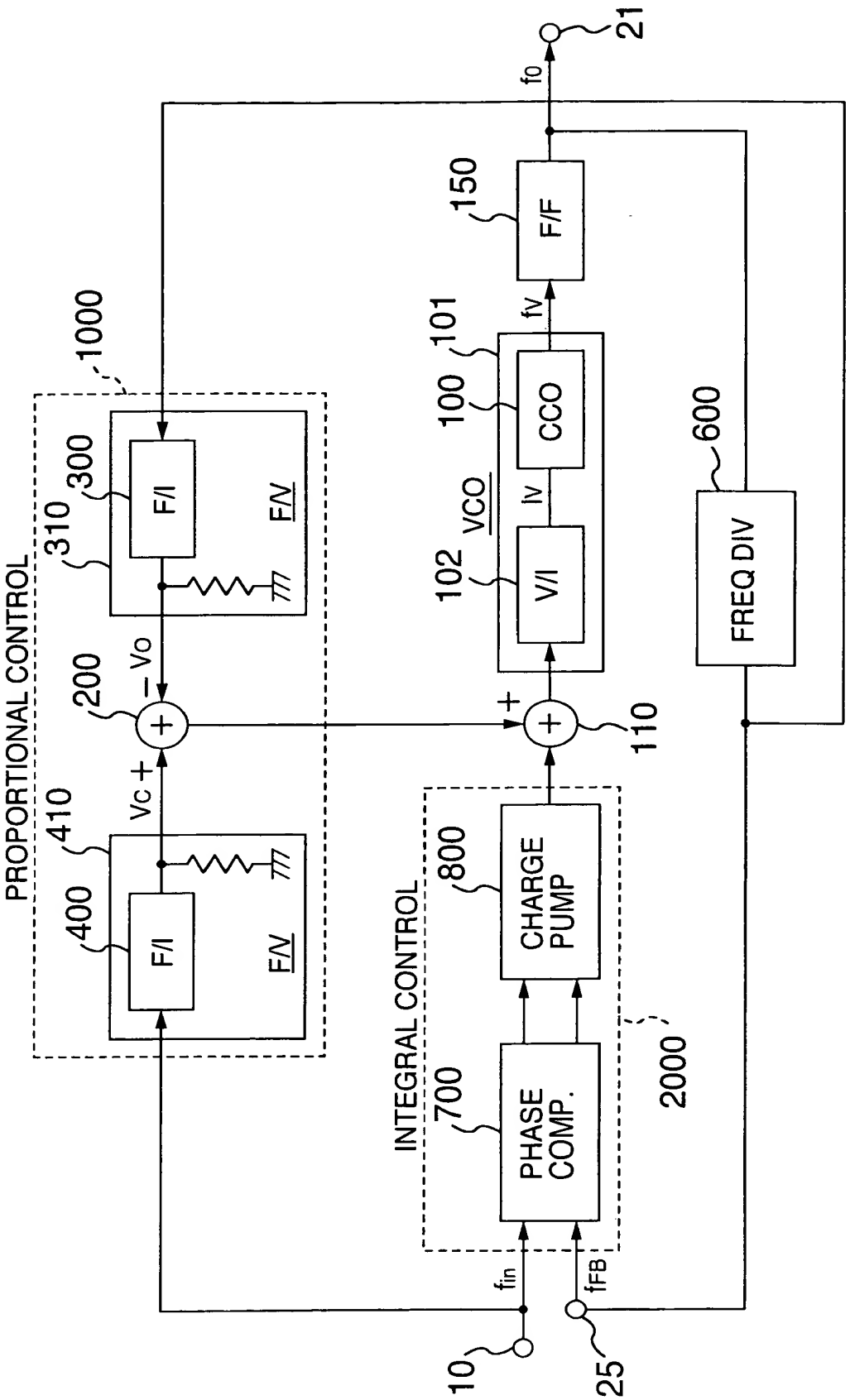
21
fo
150
F/F
101
100
CCO
fv
600
FREQ DIV
1000
300
F/I
F/V
310
VCO
102
V/I
Iv
200
− Vo
+
110
PROPORTIONAL CONTROL
410
Vc +
400
F/I
F/V
INTEGRAL CONTROL
800
CHARGE PUMP
700
PHASE COMP.
2000
fin
fFB
10
25

FIG. 13

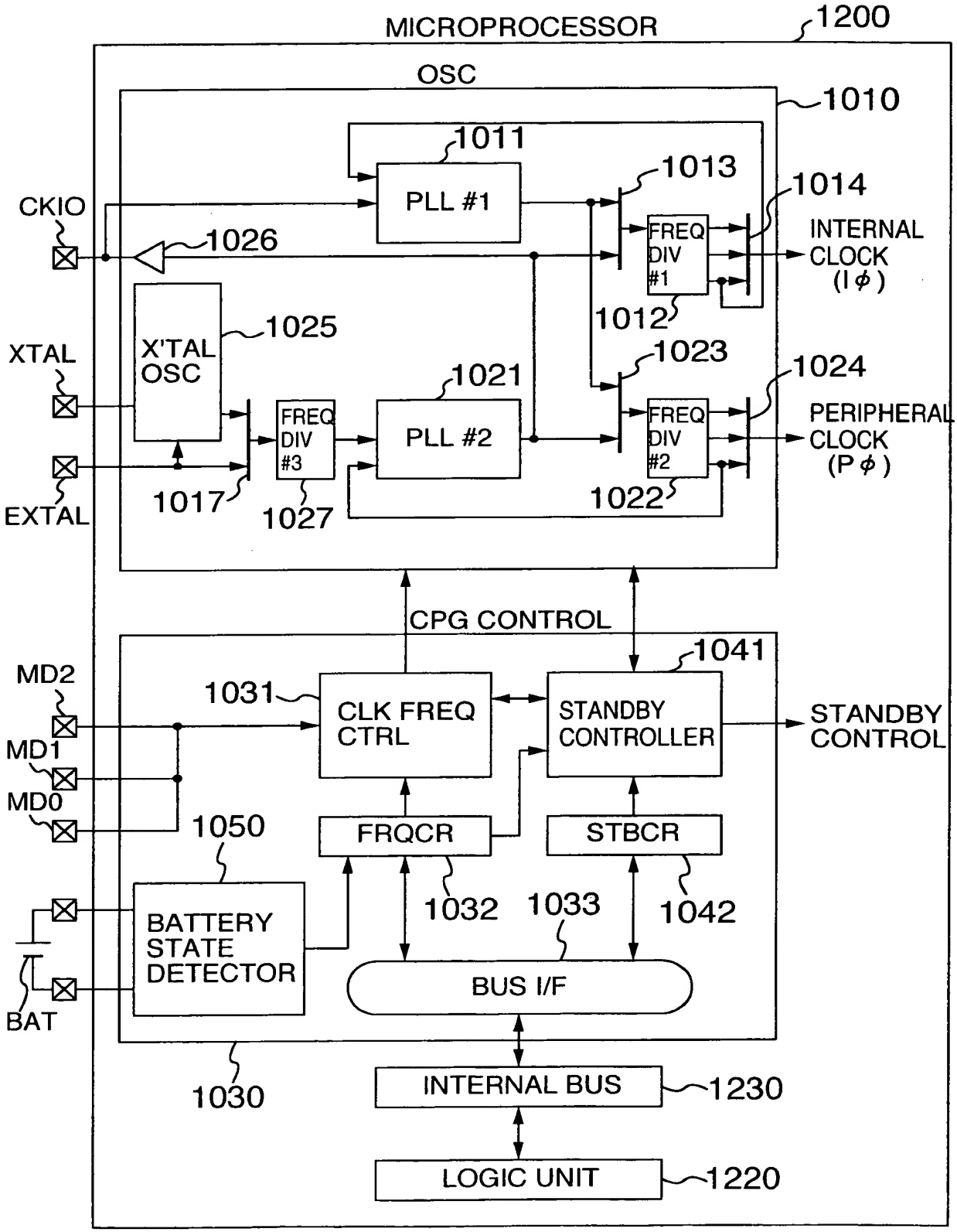
MICROPROCESSOR
1200
OSC
1010
1011
PLL #1
1013
1014
CKIO
1026
FREQ DIV #1
INTERNAL CLOCK (Iφ)
1012
X'TAL OSC
1025
XTAL
1023
1024
1021
FREQ DIV #3
PLL #2
FREQ DIV #2
PERIPHERAL CLOCK (Pφ)
EXTAL
1017
1027
1022
CPG CONTROL
1041
MD2
1031
CLK FREQ CTRL
STANDBY CONTROLLER
STANDBY CONTROL
MD1
MD0
1050
FRQCR
STBCR
1032
1033
1042
BATTERY STATE DETECTOR
BUS I/F
BAT
1030
INTERNAL BUS
1230
LOGIC UNIT
1220

FIG. 14

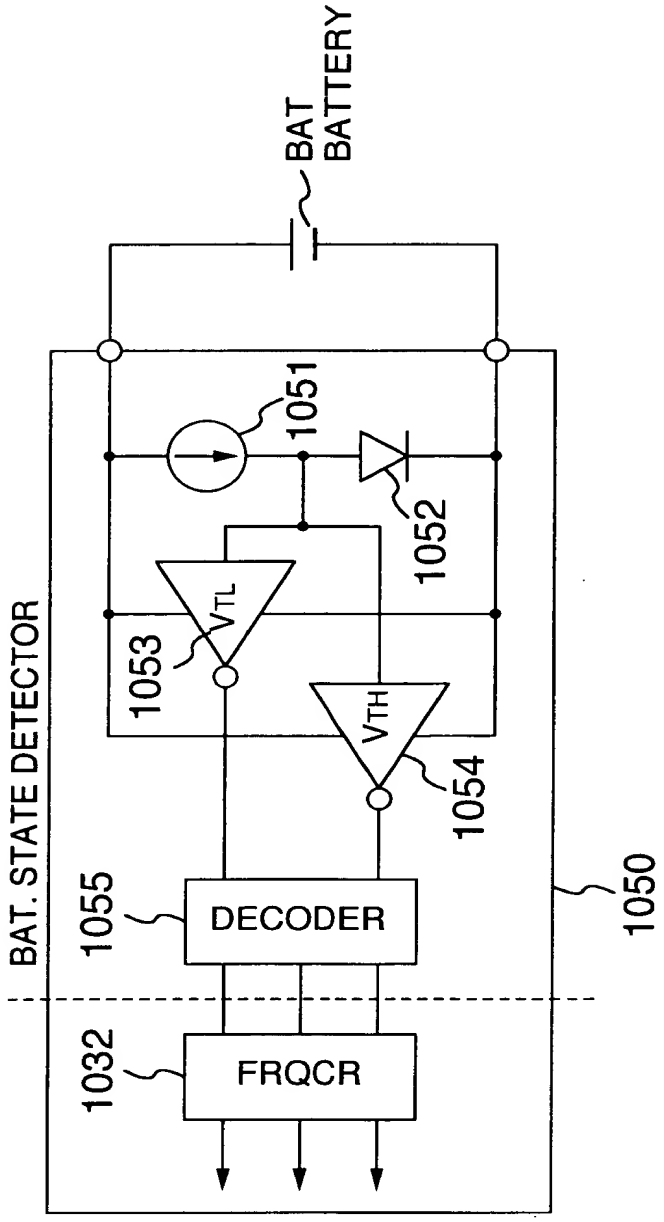
BAT
BATTERY
1051
1052
VTL
1053
VTH
1054
BAT. STATE DETECTOR
1055
DECODER
1050
1032
FRQCR

FIG. 15

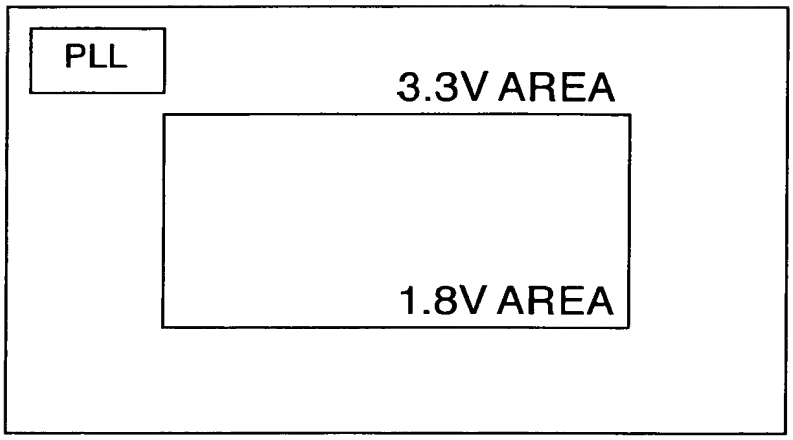

FIG. 17

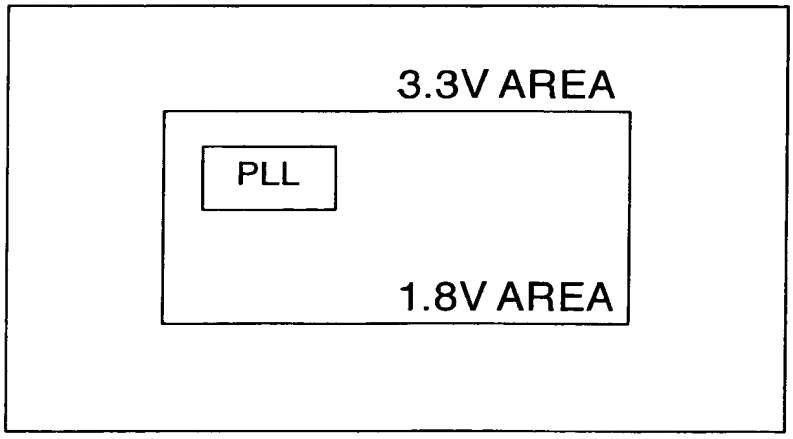

FIG. 16

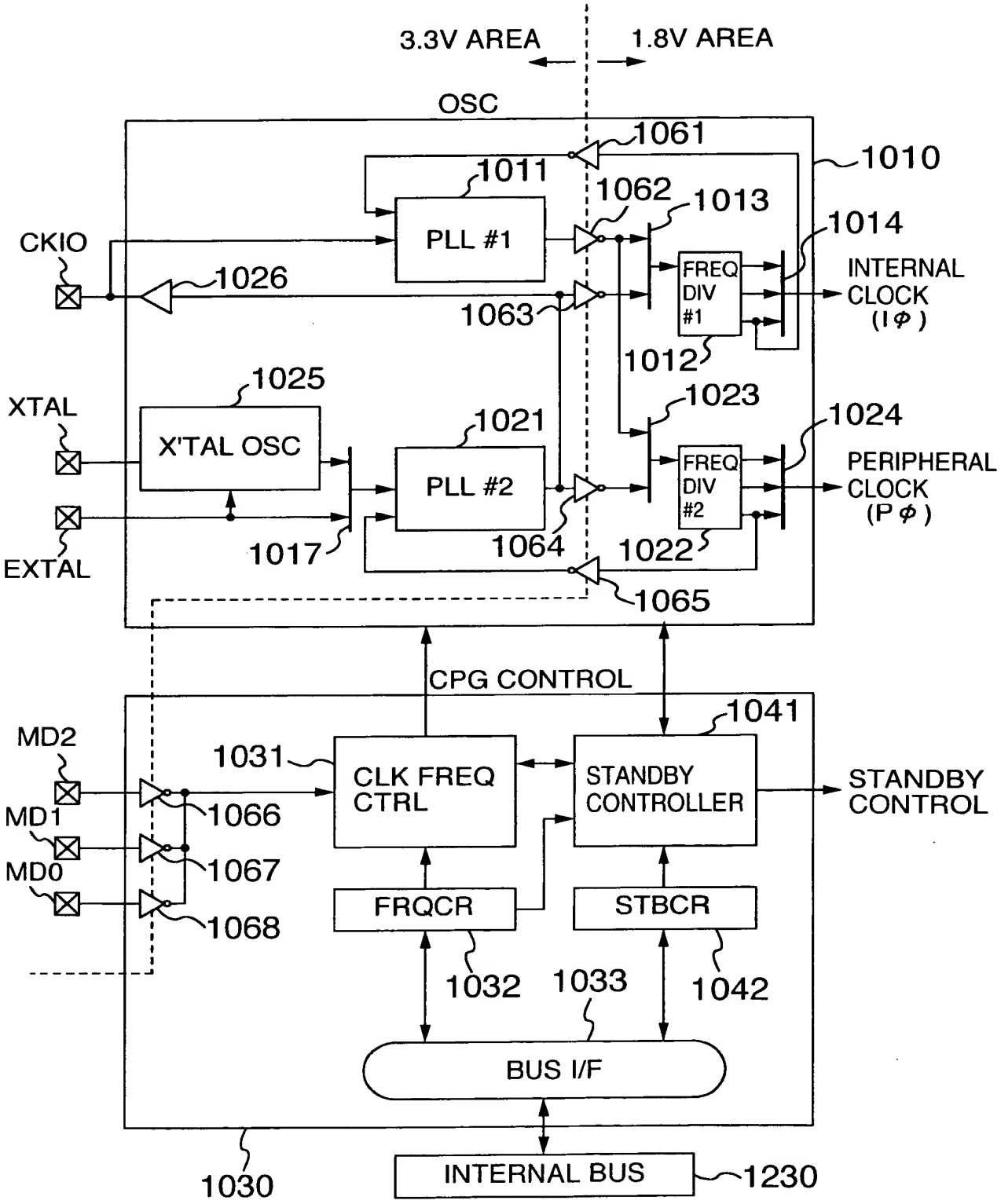
3.3V AREA
1.8V AREA
OSC
1061
1010
1011
1062
1013
1014
CKIO
PLL #1
FREQ DIV #1
INTERNAL CLOCK (IΦ)
1026
1063
1012
1025
1023
1024
XTAL
X'TAL OSC
1021
PLL #2
FREQ DIV #2
PERIPHERAL CLOCK (PΦ)
EXTAL
1017
1064
1022
1065
CPG CONTROL
1041
MD2
1031
CLK FREQ CTRL
STANDBY CONTROLLER
STANDBY CONTROL
MD1
1066
MD0
1067
1068
FRQCR
STBCR
1032
1033
1042
BUS I/F
1030
INTERNAL BUS
1230

FIG. 18

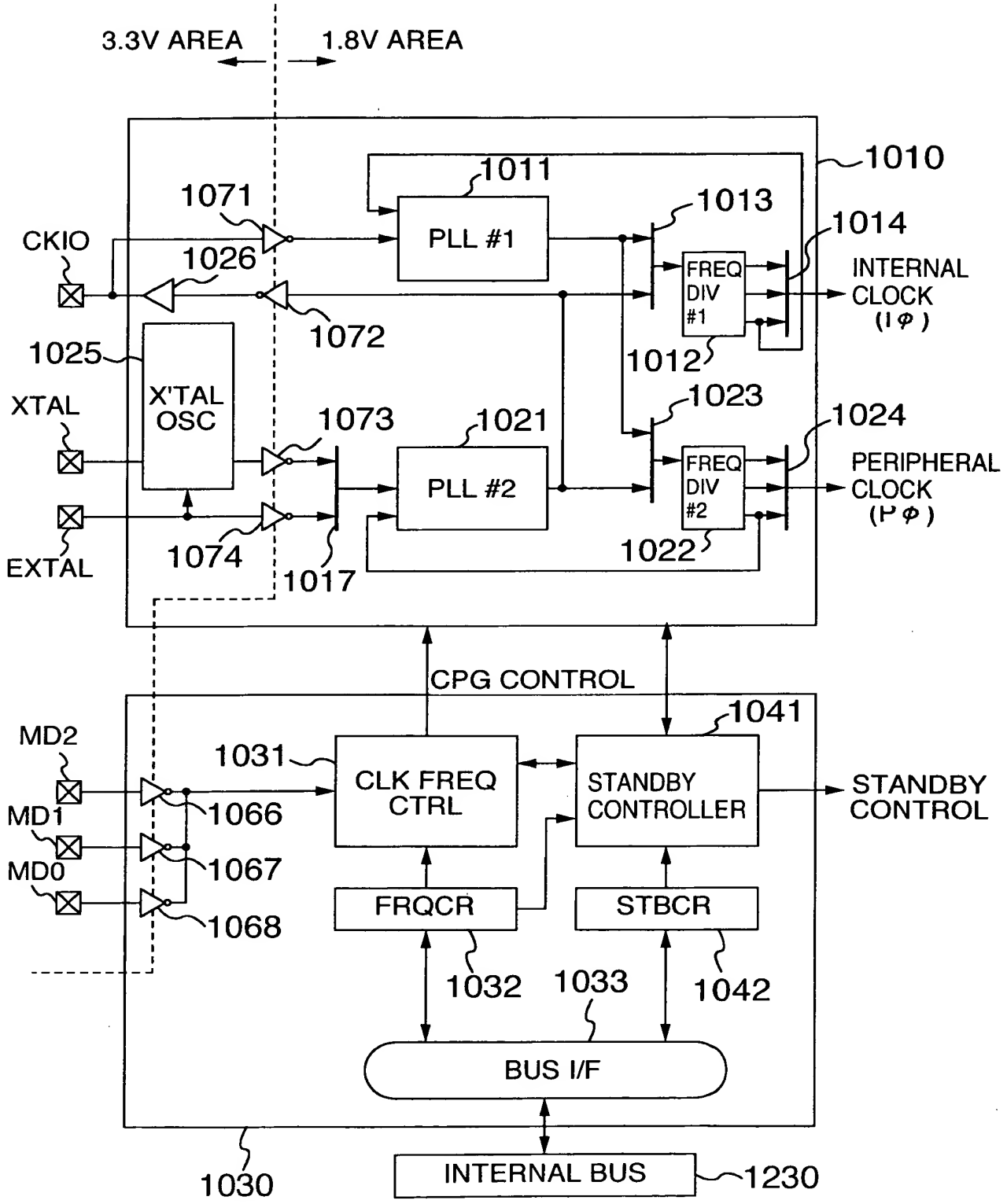
3.3V AREA
1.8V AREA
1010
1011
1071
PLL #1
1013
1014
CKIO
1026
FREQ DIV #1
INTERNAL CLOCK (IΦ)
1072
1025
1012
X'TAL OSC
1023
1024
XTAL
1073
1021
PLL #2
FREQ DIV #2
PERIPHERAL CLOCK (PΦ)
EXTAL
1074
1022
1017
CPG CONTROL
1041
MD2
1031
CLK FREQ CTRL
STANDBY CONTROLLER
STANDBY CONTROL
MD1
1066
MD0
1067
1068
FRQCR
STBCR
1032
1033
1042
BUS I/F
1030
INTERNAL BUS
1230

FIG. 19

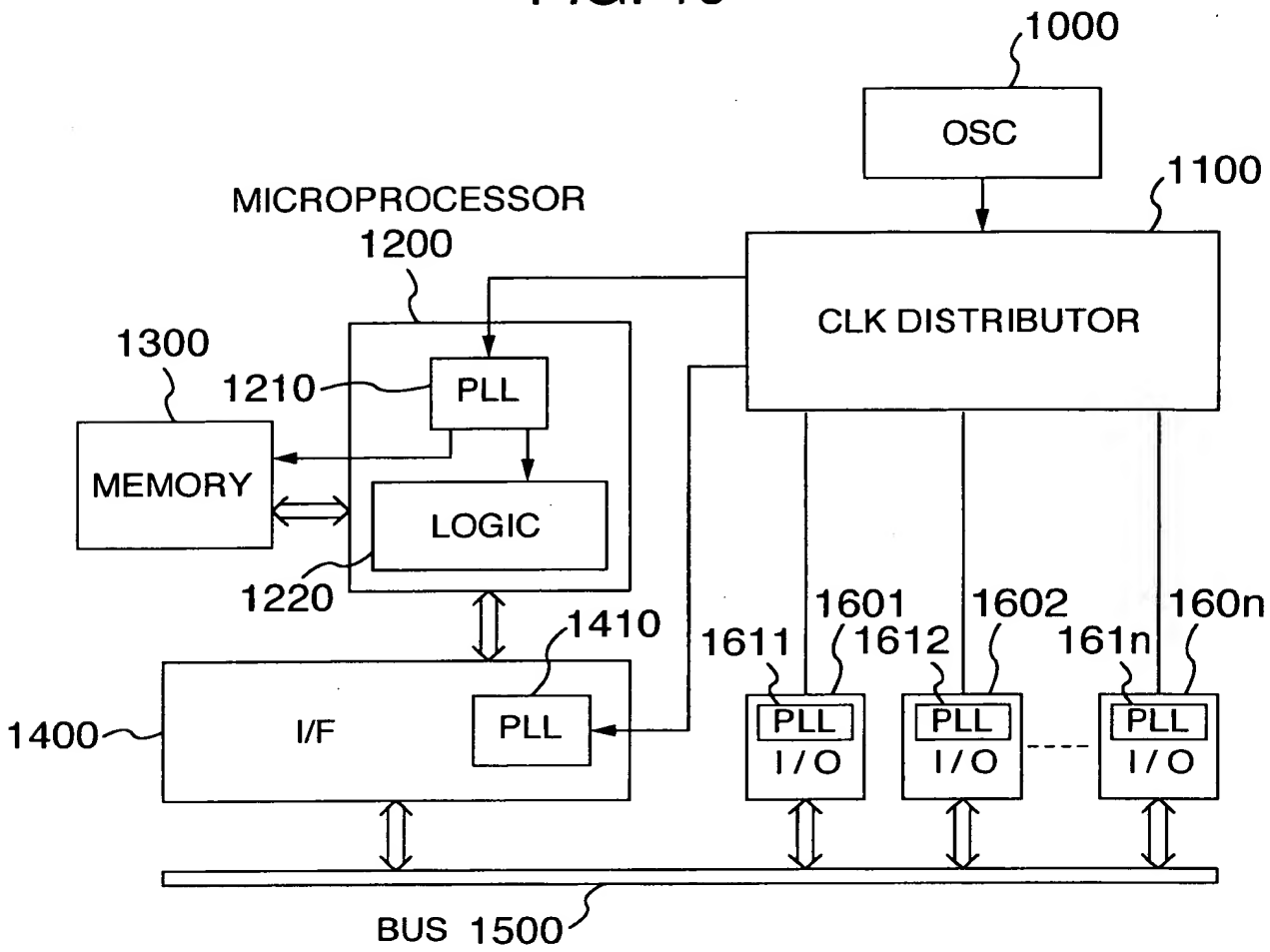
1000
OSC
1100
CLK DISTRIBUTOR
MICROPROCESSOR
1200
1300
1210
PLL
MEMORY
LOGIC
1220
1410
1400
I/F
PLL
1611
1601
1612
1602
161n
160n
PLL
I/O
PLL
I/O
PLL
I/O
BUS 1500

FIG. 20

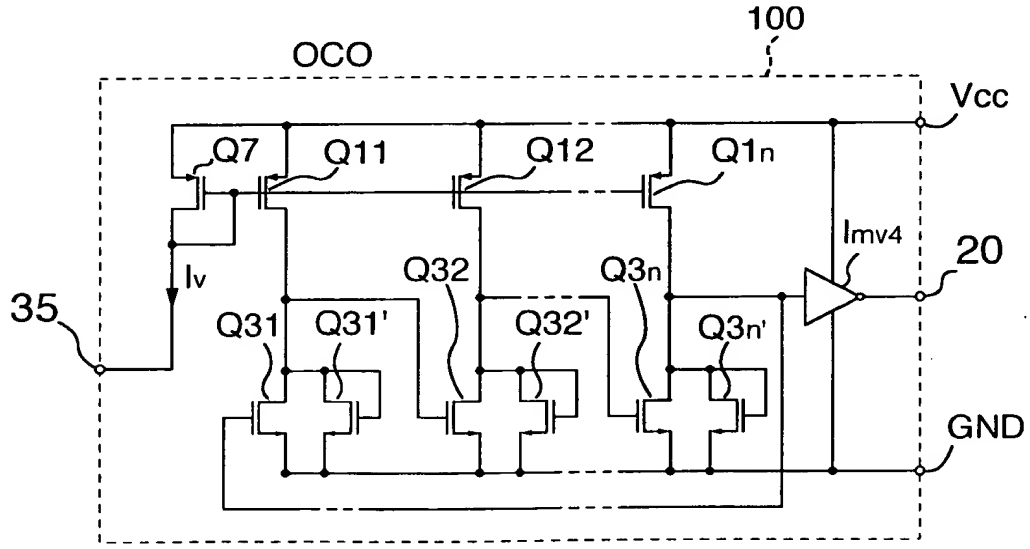
100
OCO
Vcc
Q7
Q11
Q12
Q1n
Imv4
20
Iv
Q32
Q3n
35
Q31
Q31'
Q32'
Q3n'
GND

FIG. 21

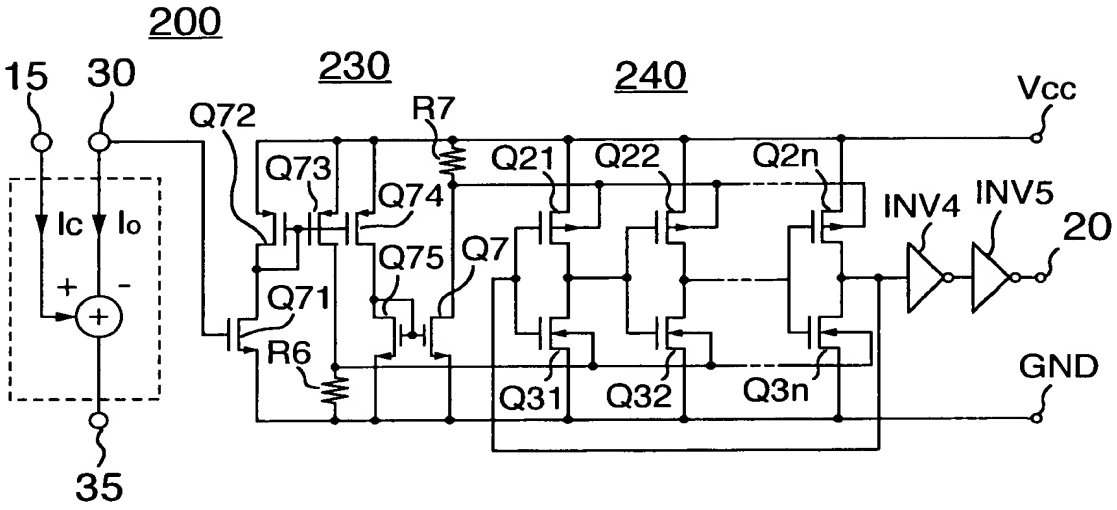
200
15
30
230
240
Vcc
Q72
R7
Q73
Q74
Q21
Q22
Q2n
INV4
INV5
20
Ic
Io
Q75
Q7
Q71
R6
GND
Q31
Q32
Q3n
35

FIG. 22

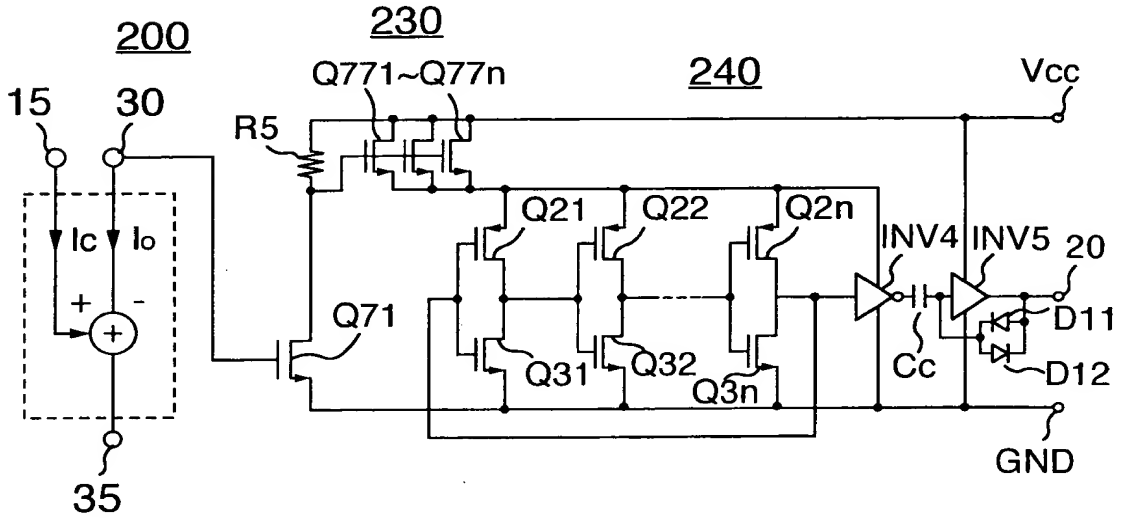
200
230
Q771~Q77n
240
Vcc
15
30
R5
Q21
Q22
Q2n
INV4
INV5
20
Ic
Io
Q71
D11
Q31
Q32
Q3n
Cc
D12
GND
35

FIG. 23

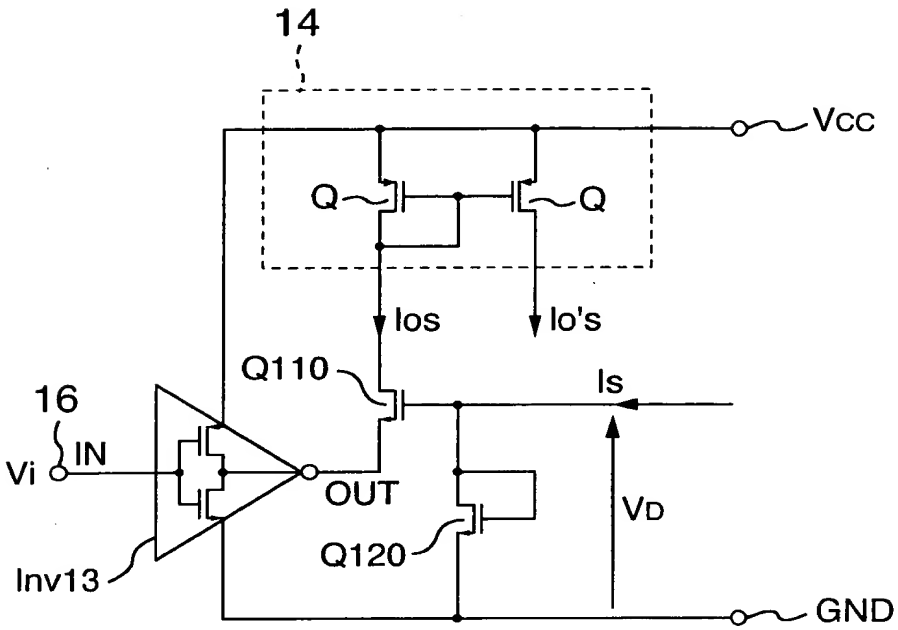
14
Vcc
Q
Q
Ios
Io's
Q110
Is
16
Vi
IN
OUT
VD
Q120
Inv13
GND

FIG. 24

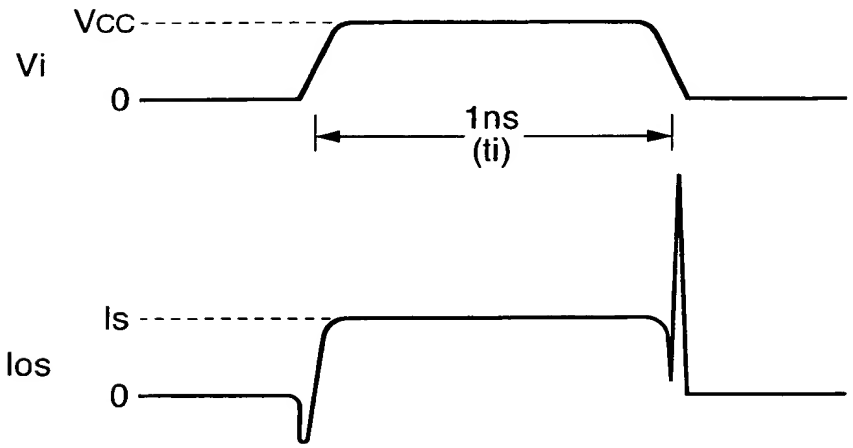
Vcc
Vi
0
1ns
(ti)
Is
Ios
0

FIG. 25

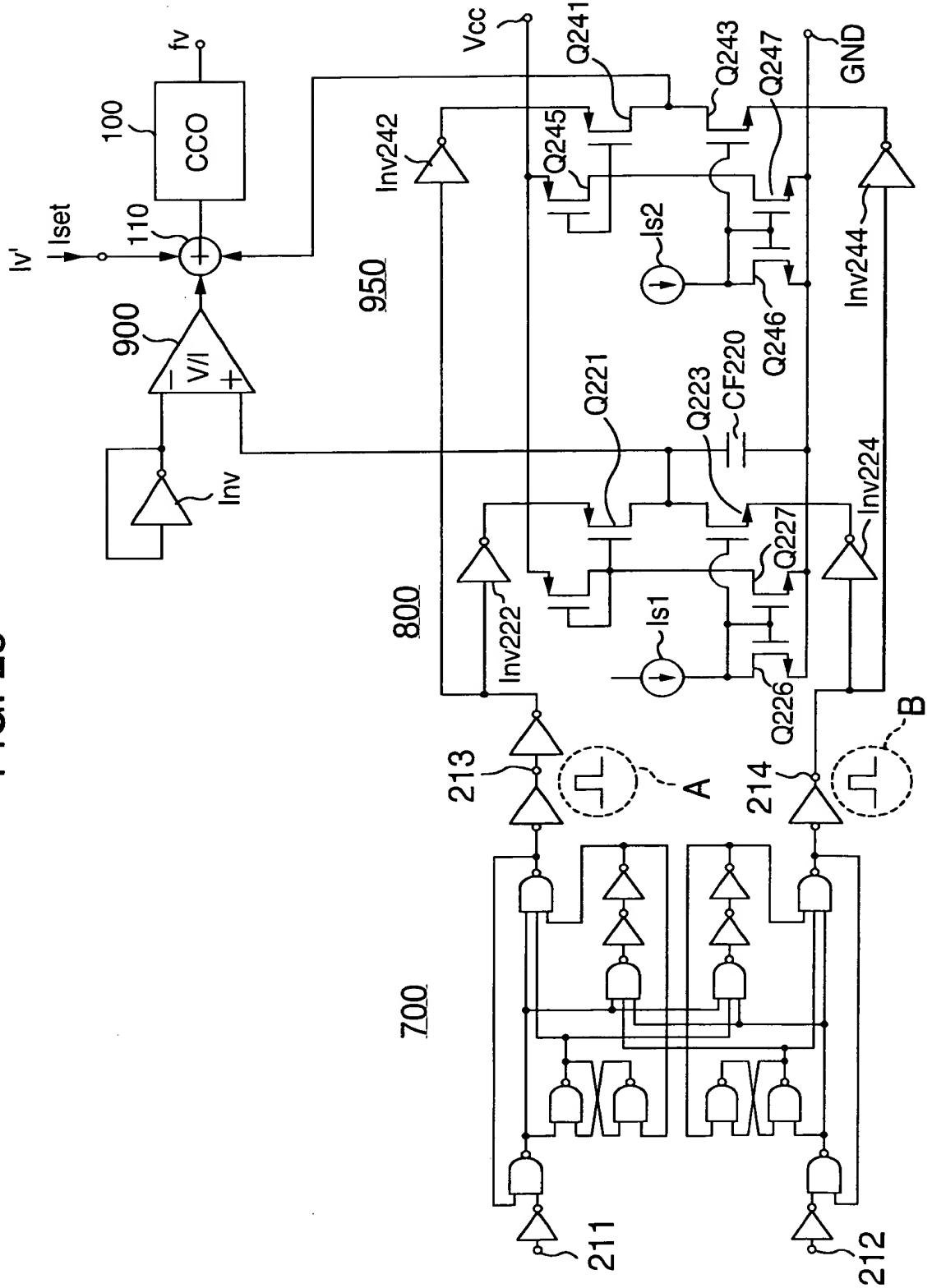
fv
100
CCO
110
Iv'
Iset
900
V/I
Inv
950
Vcc
Q241
Q243
Q247
GND
Inv242
Q245
Is2
Inv244
Q246
Q221
Q223
CF220
Inv224
800
Inv222
Q227
Is1
Q226
213
214
A
B
700
211
212

FIG. 26

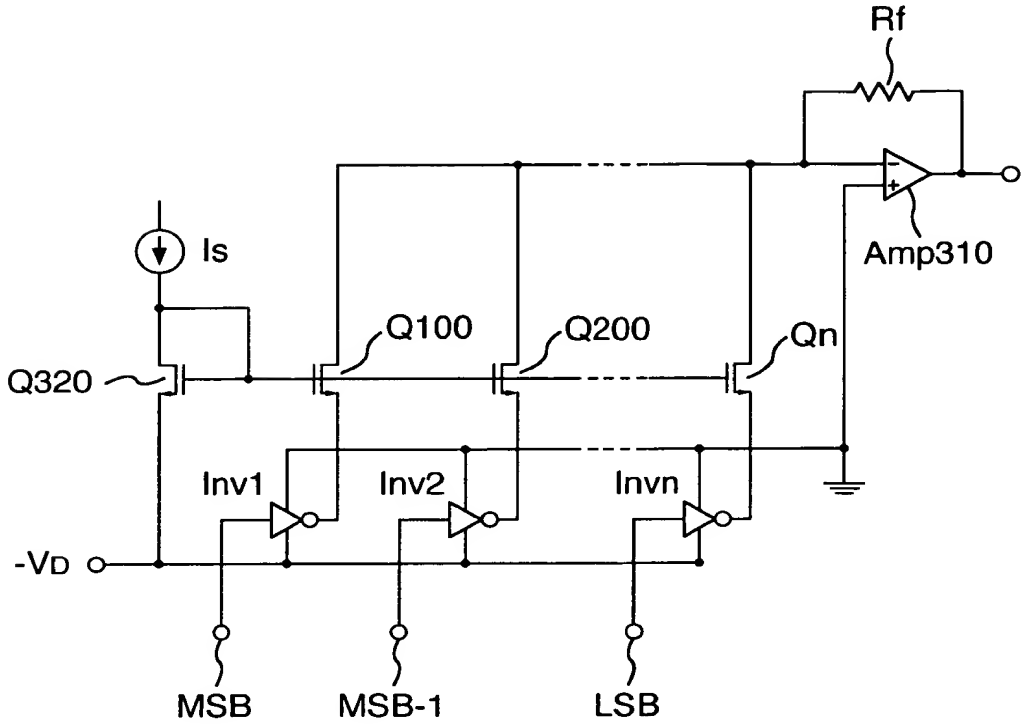
Rf
Is
Amp310
Q100
Q200
Qn
Q320
Inv1
Inv2
Invn
-VD
MSB
MSB-1
LSB

FIG. 27

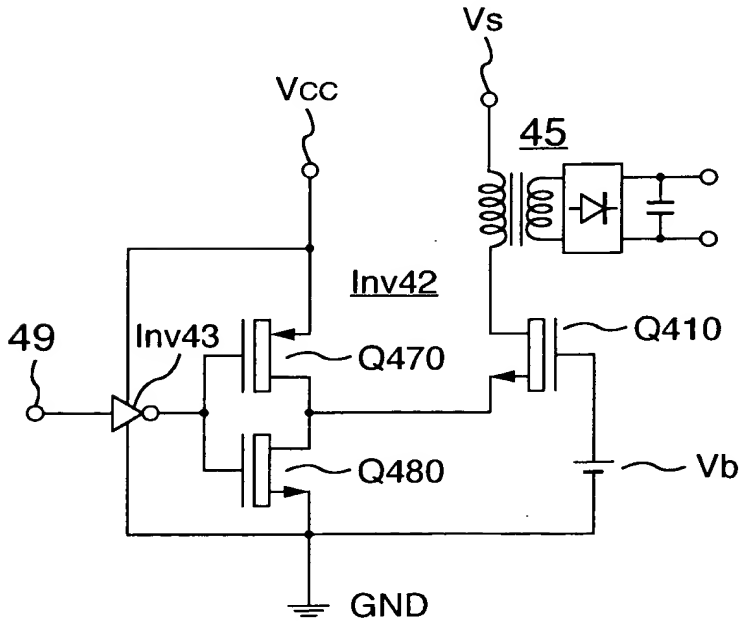
Vs
Vcc
45
Inv42
49
Inv43
Q470
Q410
Q480
Vb
GND

FIG. 28

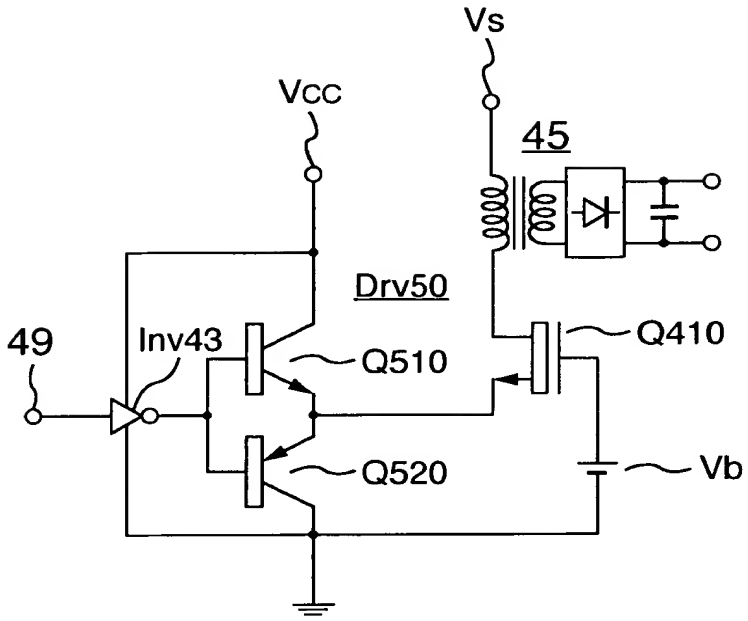
Vs
Vcc
45
Drv50
49
Inv43
Q510
Q410
Q520
Vb

FIG. 29

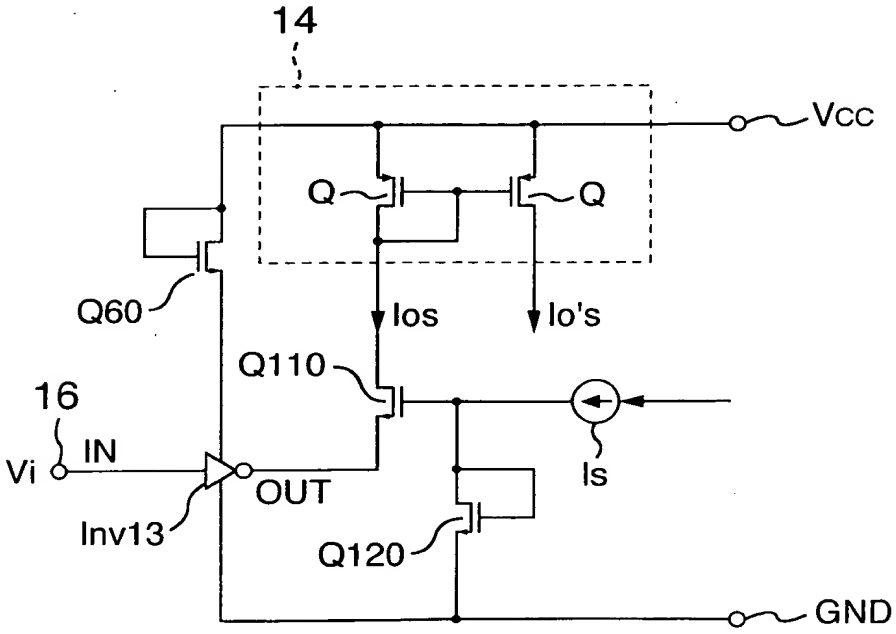
14
Vcc
Q
Q
Q60
Ios
Io's
Q110
16
Vi
IN
OUT
Is
Inv13
Q120
GND

FIG. 30